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LOW-POWER COMPILER-PROGRAMMABLE MEMORY WITH FAST ACCESS TIMING

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BACKGROUND

Field of the Disclosure

[0001] The present disclosure relates generally to integrated circuit memories, and more particularly to a memory having a low power read cycle and fast access timing.

Description of the Related Art

[0002] With today's information systems, it is preferable to minimize the power consumed by a memory device utilized in the information system. A low power memory device is especially desirable in battery powered systems or systems susceptible to over-heating. Another desirable feature for memory devices is reduced access time. Reducing the access time of a memory device enables a system utilizing the memory device to operate at faster speeds. However, these two desirable features are in conflict with each other. For example, in conventional memory devices, reducing power consumption typically increases the memory access time.

[0003] Providing a memory device that consumes less power and has fast access times is further complicated when providing compilable memory. Compilable memory refers to a memory module provided, for example, in a computer aided design (CAD) environment that allows a designer to select a physical size of a memory array during the design of an application specific integrated circuit (ASIC). Because an implemented memory module can vary in physical size, for example from 256 words to 64k words, the memory module should advantageously scale access times appropriately.What is desirable is a memory device that is low power, has fast access times and can be efficiently provided as compilable memory.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present disclosure may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0006] FIG. 1 illustrates, in block diagram form, a memory in accordance with the present invention.

[0007] FIG. 2 illustrates, in schematic diagram form, a representative portion of the memory array of the memory of FIG. 1.

[0008] FIG. 3 illustrates, in schematic diagram form, a portion of the discharge and column decode and speed-up precharge and bit line decode circuits of the memory of FIG. 1.

[0009] FIG. 4 illustrates, in schematic diagram form, the differential sense amplifier of FIG. 1.

[0010] FIG. 5 illustrates a timing diagram illustrating the operation of the memory of FIG. 1 according to an embodiment of the present disclosure.

[0011] FIG. 6 illustrates, in schematic diagram form, the timing circuit of FIG. 1.

[0012] FIG. 7 illustrates, in schematic diagram form, the delay unit of FIG. 6.

[0013] FIG. 8 illustrates, in schematic diagram form, an exemplary delay stage of FIG. 7.

[0014] FIG. 9 illustrates an exemplary scatter plot illustrating access times for a variety of charging pulse widths and sense delays according to an embodiment of the present disclosure.

[0015] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0016] A low-power, compilable memory using a charging pulse technique to improve access times over other low-power memory implementations is provided. The memory includes circuitry configured to discharge a plurality of bit lines during an inactive memory access period to reduce power consumption. The memory also includes other circuitry that applies a charging pulse during an active memory access period on a select one of the plurality of bit lines prior to sensing a voltage difference between the select one of the plurality of bit lines and a reference signal in order to improve the memory access times. The memory includes a two stage timing circuit to control the duration of the charging pulse and the enabling of a sense amplifier. An automatic memory compiler adjusts the timing circuit during memory design. The memory compiler provides a programmable physical size of the memory and optimizes the access timing while ensuring reliable sensing. The compiler calculates timing for the two stage timing circuit according to a mathematical formula that provides for highly accurate and predicable access time delays for multiple memory configurations.

[0017] FIG. 1 illustrates, in block diagram form, a memory 100 in accordance with one embodiment of the present invention. In the illustrated embodiment, memory 100 is a mask programmable read only memory (ROM). However, in other embodiments, memory 100 may be another memory type. Memory 100 includes a plurality of memory arrays including memory arrays 102 and 104. Note that although two memory arrays are illustrated in FIG. 1, more memory arrays and corresponding discharge and data line decode circuits may be present in other embodiments. For example, in memory 100 there are 8 memory arrays. In another embodiment, there can be more or less than 8 memory arrays.

[0018] Discharge and first level column decode circuit 106 is coupled to memory array 102 and discharge and first level column decode circuit 108 is coupled to memory array 104. Discharge and first level column decode circuits 106 and 108 function to both control bit line discharge during inactive memory access periods and the coupling of a bit line to speed-up precharge and bit line decode 112 in response to a column decode signal PREMUX via a data line labeled DLA[0] or DLA[7], respectively, during active memory access periods.

[0019] Speed-up precharge and bit line decode 112 precharges a selected one of the data lines, such as for example, data line DLA[0] in response to speed-up precharge signal PULLUP during active memory access periods. Speed-up precharge and bit line decode 112 couples data line DLA[0] to sense amplifier 124 in response to a column decode signal labeled POSTMUX. The decoded bit line is precharged by the precharging of the decoded data line.

[0020] Reference circuit 120 also receives speed-up precharge signal PULLUP and column address signal POSTMUX and provides a reference current REF to sense amplifier 124 during a read cycle of memory 100.

[0021] Sense amplifier 124 has input/output terminals for receiving reference signal REF and a data line signal labeled DL. During a read cycle of memory 100, sense amplifier 124 compares reference current REF to data line current DL to determine the logic state of a selected memory location. Buffer 128 is coupled to data line DL and reference line REF and receives a data signal corresponding to the state of the selected memory location. In response, buffer 128 provides a buffered data out signal labeled DATA OUT. Buffer 128 can contain a latching circuit to store data for the remainder of a cycle, once sense amplifier 124 has sensed the DL/REF differential.

[0022] Timing circuit 130 provides accurate timing for the PULLUP and SENSE signals. The duration of the charging pulse PULLUP is controlled such that the DL and REF nodes are first drawn to a midpoint voltage. The enabling of a sense amplifier is delayed from the end of the PULLUP charging pulse to allow sufficient time for the DL and REF nodes to separate towards their DC levels unassisted. The width of PULLUP signal and the delay between PULLUP becoming inactive and SENSE becoming active (the self timing delay) are finely tuned to balance the need for fast access times and the need to allow the signals to properly reflect the value stored in the memory.

[0023] FIG. 2 illustrates, in schematic diagram form, a representative portion of memory array 102 of memory 100 of FIG. 1. Memory array 102 includes a plurality of word lines, including word lines labeled WL[0] through WL[N], extending in one direction. A plurality of bit lines, including bit lines labeled BL[0] through BL[N], extends in another direction across the word lines. Memory array 100 is a mask

programmable ROM and a transistor, such as for example transistor 226, is coupled to a word line and a bit line at predetermined intersections of the word lines and bit lines depending on the particular data being stored in memory array 102. In the illustrated embodiment, a transistor is located at address locations that are intended to provide a low logic state corresponding to a logic "0" when read. Locations that do not have a transistor will be read as a high logic state corresponding to a logic "1" when read. By way of example, transistor 226 has a gate coupled to a word line labeled WL[2], a drain coupled to bit line BL[6], and a source coupled to V_{SS}. The other transistors are connected to the bit lines and word lines randomly and are not intended to reflect any particular data. In the illustrated embodiment, V_{SS} is coupled to ground potential and V_{DD} is coupled to a positive supply voltage, such as for example 1.5 volts. Note that memory array 100 is illustrated as a diffusion ROM. One skilled in the art will recognize that the present disclosure can beneficially be applied to other types of memory arrays, for example, contact ROM arrays.

[0024] FIG. 3 illustrates, in schematic diagram form, a portion of the discharge and first level column decode 106 and speed-up precharge and bit line decode 112 circuits of the memory of FIG. 1. Column decode transistors 304[7:0] receive one of first level column decode signals PREMUX[7:0], respectively. In addition, the inverses of PREMUX[7:0], that is, PREMUXB[7:0], are provided to discharge NMOS transistors 306[7:0], respectively. In the illustrated embodiment, discharge transistors 306[7:0] are coupled to corresponding bit lines BL[7:0] of memory array 102 in FIG. 2 in response to deasserted column decode signals PREMUX[7:0], for example, during inactive memory access periods. Discharge transistor 306[7] has a drain coupled to bit line BL[7], a gate coupled to PREMUXB[7], and a source coupled to V_{SS}. When inactive, POSTMUX signal drives inverter 318 which drives discharge NMOS transistor 320, discharging node DLA. Thus, all bit lines BL[7:0] and the DLA node are discharged low before a read operation begins.

[0025] During an active memory access period, one of bit lines BL[7:0] is coupled to data line DLA when a corresponding one of the column decode signals PREMUX[7:0] is asserted. Data line DLA is coupled to data line DL via transistor 308 in response to column decode signal POSTMUX being asserted. Column decode signal POSTMUX is the second level of column decoding. Transistor 308 has a first

drain/source terminal connected to data line DLA, a second drain/source terminal connected to data line DL, and a gate coupled to receive second level column decode signal POSTMUX. PULLUP signal becomes active for a specified amount of time at the beginning of a read cycle, enabling pullup NMOS transistor 312 through NAND gate 314 and inverter 316. When active, a POSTMUX signal enables pass gate NMOS transistor 308. When a read operation begins, only one of discharge transistors 306[7:0] turn off while the others remain active, and the corresponding one of pass gates 304[7:0] and pass gate 308 turn on. The selected bit line and node DL are pulled towards Vss due to discharged bit line capacitance. To decrease the effect of the discharge capacitance and the time required for node DL to rise towards its DC level (for sensing a logic "1"), the PULLUP signal having a programmable pulse width brings node DLA to a midpoint voltage, for example, Vdd/2, provided through transistor 312, and decoded through NAND gate 314 and inverter 316. Following the pull-up, a short self-timing delay occurs prior to enabling the sense amplifier to allow, for example, approximately 100 mV of differential to occur between nodes DL and REF.

[0026] FIG. 4 illustrates, in schematic diagram form, the differential sense amplifier of FIG. 1. The sense amplifier includes cross-coupled latch 414, P-channel transistors 416, 418, 424, and 426, N-channel transistors 420 and 422, and inverters 428, 430, and 432. Cross-coupled latch 414 includes a pair of conventional cross-coupled inverters. P-channel transistors 416 and 418 and N-channel transistors 420 and 422 couple cross-coupled latch 414 to V_{DD} and Vss, respectively, in response to a logic high sense enable signal SENSE. Inverters 428, 430, and 432 are used to invert the logic level of sense enable signal SENSE to make P-channel transistors 416, 418, 424, and 426 conductive from the logic high sense enable signal SENSE. Nodes 434 and 436 function as both input and output terminals for cross-coupled latch 414. P-channel transistors 424 and 426 provide current sources for the reference line and the data line during a read cycle.

[0027] The differential voltage between the multiplexed bit line (DL) and the reference line (REF) is detected by sense amplifier 400, and converted to a logic "0" or "1", which is registered and passed to an output driver.

[0028] For stability and reliability, the sense signal is configured to enable the sense amplifier to sense when, for example, 100 mV of differential has been developed between nodes DL and REF. The timing delay can allow for 100 mV, 150 mV, 200 mV or any other differential reliably sensed by the sense amplifier.

[0029] FIG. 5 illustrates a timing diagram illustrating the operation of the memory of FIG. 1 according to an embodiment of the present disclosure. As illustrated at time 501, DL and REF signals are pulled low towards Vss when the word line becomes active due to the discharge capacitance of their respective memory array bit lines. At time 502, PULLUP signal becomes active, drawing nodes DL and REF up toward a midpoint voltage. At time 503, PULLUP signal becomes inactive allowing nodes DL and REF to separate towards their DC levels unassisted. At time 504, SENSE signal becomes active, enabling the sense amplifier to sense the difference between DL and REF signals. The width of PULLUP signal and the delay between PULLUP becoming inactive and SENSE becoming active (the self timing delay) are finely tuned to balance the need for fast access times and the need to allow the signals to properly reflect the value stored in the memory. For compilable memory, the pulse width of PULLUP signal and the self-timing delay is programmable.

[0030] FIG. 6 illustrates, in schematic diagram form, the timing circuit 130 of FIG. 1. Programmable values PVAL[5:0] and RVAL[5:0] control the duration of the charging pulse PULLUP and the enabling of a sense amplifier circuit (the self timing delay). Delay unit 602 sets the width of the bit line PULLUP pulse. Delay unit 604 adds additional delay before triggering the sense amplifier to ensure, for example, at least 100 mV of differential between the DL and REF signals. Pulse width unit 606 sets the width of the sense amplifier trigger signal SENSE to ensure that data is reliably sensed and registered.

[0031] During the design of memory using, for example, a CAD tool, a user selects a physical memory size. The CAD tool subroutine calculates appropriate values for PVAL[5:0] and RVAL[5:0] to provide optimal access timing.

[0032] FIG. 7 illustrates, in schematic diagram form, the delay unit of FIG. 6 (delay unit 604 or 606). The delay unit has, for example, six delay stages 702, 704, 706, 708, 710, 712. Each delay stage includes a delay path and a non-delay path. A

control input signal (D5, D4, D3, D2, D1 or D0) sent to each delay stage controls the selection between the delay path and the non-delay path. For example, if the control input signal Dn is a logic zero, the input to output signal goes through the non-delay path. If the control input signal Dn is a logic one, the input to output signal goes through the delay path. The number of elements in (and therefore the delay of) the non-delay path is the same in each of the six stages. The number of elements in the delay path of each delay stage varies as described below.

[0033] FIG. 8 illustrates, in schematic diagram form, an exemplary delay stage of FIG. 7. The delay path of this exemplary delay stage includes six elements, NAND 802, NAND 804, NAND 806, NAND 808, NAND 810 and NAND 816. The non-delay path (which is the same in all six stages) includes two elements, NAND 814 and NAND 816. Inverter 812 aids in the selection of the delay or non-delay path.

[0034] The number of NAND elements in the delay path varies amongst the six delay stages. The delay path includes an intrinsic delay portion including NAND elements 802, 808, 810 and 816. The intrinsic delay portion is the same for each of the six delay stages. The delay path also includes a varying delay portion 618 which include a varying number of NAND pairs from 0 to 31 amongst the six delay stages. In one embodiment of the present disclosure, delay stage 702 includes zero NAND pairs in varying delay portion 618, delay stage 704 includes one NAND pair in varying delay portion 618, delay stage 706 includes three NAND pairs in varying delay portion 618, delay stage 708 includes seven NAND pairs in varying delay portion 618, delay stage 710 includes 15 NAND pairs in varying delay portion 618, and delay stage 712 includes 31 NAND pairs in varying delay portion 618.

[0035] The following table illustrates how the total number of NAND gates through which the input signal must pass varies by control value, which likewise controls the input to output delay of the signal.

TABLE 1.

CONTROL VALUE D[5:0]	DELAY STAGE 712 NANDs (66 or 2)	DELAY STAGE 710 NANDs (34 or 2)	DELAY STAGE 708 NANDs (18 or 2)	DELAY STAGE 706 NANDs (10 OR 2)	DELAY STAGE 704 NANDs (6 OR 2)	DELAY STAGE 702 NANDs (4 OR 2)	TOTAL NANDS
000000	2	2	2	2	2	2	12
000001	2	2	2	2	2	4	14
000010	2	2	2	2	6	2	16
000011	2	2	2	2	6	4	18
000100	2	2	2	10	66	2	20
000101	2	2	2	10	66	4	22
000110	2	2	2	10	6	2	24
000111	2	2	2	10	6	4	26
001000	2	2	18	2	2	2	28
001001	2	2	18	2	2	4	30
001010	2	2	18	2	6	2	32
001011	2	2	18	2	6	4	34
001100	2	2	18	10	66	2	36
001101	2	2	18	10	66	4	38
001110	2	2	18	10	6	2	40
001111	2	2	18	10	6	4	42
010000	2	34	2	2	2	2	44
010001	2	34	2	2	2	4	46
010010	66	34	2	2	6	2	48
010011	66	34	2	2	6	4	50
010100	66	34	2	10	66	2	52
010101	2	34	2	10	66	4	54
010110	2	34	2	10	6	2	56
010111	2	34	2	10	6	4	58
011000	2	34	18	2	2	2	60
011001	2	34	18	2	2	4	62
011010	2	34	18	2	6	2	64
011011	2	34	18	2	6	4	66
011100	2	34	18	10	66	2	68
011101	2	34	18	10	66	4	70
011110	2	34	18	10	6	2	72
011111	2	34	18	10	6	4	74
100000	66	2	2	2	2	2	76
100001	66	2	2	2	2	4	78
100010	66	2	2	2	6	2	80
100011	66	2	2	2	6	4	82
100100	66	2	2	10	66	2	84
100101	66	2	2	10	66	4	86
100110	66	2	2	10	6	2	88
100111	66	2	2	10	6	4	90
101000	66	2	18	2	2	2	92
101001	66	2	18	2	2	4	94
101010	66	2	18	2	6	2	96
101011	66	2	18	2	6	4	98

101100	66	2	18	10	66	2	100
101101	66	2	18	10	66	4	102
101110	66	2	18	10	6	2	104
101111	66	2	18	10	6	4	106
110000	66	34	2	2	2	2	108
110001	66	34	2	2	2	4	110
110010	66	34	2	2	6	2	112
110011	66	34	2	2	6	4	114
110100	66	34	2	10	66	2	116
110101	66	34	2	10	66	4	118
110110	66	34	2	10	6	2	120
110111	66	34	2	10	6	4	122
111000	66	34	18	2	2	2	124
111001	66	34	18	2	2	4	126
111010	66	34	18	2	6	2	128
111011	66	34	18	2	6	4	130
111100	66	34	18	10	66	2	132
111101	66	34	18	10	66	4	134
111110	66	34	18	10	6	2	136
111111	66	34	18	10	6	4	138

[0036] Referring to the above table, in the exemplary embodiment the input to output delay passes through as few as 12 to as many as 138 NAND gates. One skilled in the art will recognize that alternate embodiments can use various number of delay stages and number of delay elements to provide differing delay ranges.

[0037] Note that in FIG. 8 that all logic gates in the delay path are NAND gates. This enables more accuracy in matching delay paths. Also, note that in the non-delay path, the input signal flows through the upper input on NAND 814 and the lower input of NAND 816. In the delay path, the input signal flows through the upper input of NAND 810 and the lower input on NAND 808. Because the upper/lower input delays can vary, the upper/lower inputs of the non-delay path mimic the delay path, helping to ensure linear delay increments across the full range of binary control counts.

[0038] A memory compiler can be fully automated to build any customer-determined configuration (within the compiler limits). The values of PVAL and RVAL can be hard wired based upon the specified configuration. Mathematical equations are needed to determine the PVAL and RVAL binary numbers to ensure sufficient sense amplifier differential, combined with the fastest access times possible, for all PVT points.

[0039] FIG. 9 illustrates an exemplary scatter plot illustrating access timing for a variety of charging pulse widths and sense delays utilized to generate mathematical equations for the determination of PVAL and RVAL. Simulations were performed using a five by five matrix of pulse width values (PVAL) versus self-timing delay values (RVAL) numbers for 256, 512, 1024, 1536 and 2048 rows of memory. Thousands of predicted values were generated to find ranges of points with nearly equal responses for ~100 mV differential at the fastest access times. Multivariate regression analysis on the simulation results can be used to generate mathematical equations for access time and sense amplifier differential. Although the spread of the optimum equivalency distributions is not linear as the number of rows is varied, a linear response can be drawn through all five groups from which linear predictor equations for PVAL and RVAL values can be derived. For example, mathematical equations can be a follows:

$$PVAL = -3.714 + 0.015 * rows$$

$$RVAL = -2.429 + 0.009 * rows$$

[0040] As the compiler builds a memory array, the equations determine the settings for PVAL[5:0] and RVAL[5:0] for optimum differential and access time.

[0041] It should be understood that the specific steps indicated in the methods herein may be implemented in hardware and/or software. For example, a specific step may be performed using software and/or firmware executed on one or more processing modules. In general, a system for providing images may include a more generic processing module and memory. The processing module can be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcontroller, digital processor, microcomputer, a portion of the central processing unit, a state machine, logic circuitry, and/or any device that manipulates the signal. The manipulation of these signals is generally based upon operational instructions. The memory may be a single memory device or a plurality of memory devices. Such a memory device may be a read only memory, a random access memory, a floppy disk memory, magnetic tape memory, erasable memory, a portion of a system memory, and/or any device that stores operational instructions in a digital format. Note that when the processing module implements one or more of its

functions to be a state machine or logic circuitry, the memory storing in the corresponding operational instructions is embedded within the circuitry comprising the state machine and/or other logic circuitry. For example, such a system may be a circuit design tool having a compilable memory unit to facilitate implementation of memories as described herein.

[0042] The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments that fall within the true spirit and scope of the present invention. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.